Semiconductor component with a praseodymium oxide dielectric

Cross Reference to Related Applications

This application is for entry into the U.S. national phase under §371 for International Application No. PCT/EP03/10625 having an international filing date of Sept. 24, 2003, and from which priority is claimed under all applicable sections of Title 35 of the United States Code including, but not limited to, Sections 120, 363 and 365(c), and which in turn claims priority under 35 USC §119 to German Patent Application No. 102 45 590.2-33 filed on Sept. 26, 2002.

Technical Field

The invention concerns a semiconductor component with a silicon-bearing layer and a praseodymium oxide layer. The invention further concerns a process for the production of such an electronic component.

Background Art

Pr_2O_3 layers on Si(001) substrates, because of their comparatively high dielectric constant ($k \approx 30$), are particularly suitable for replacing the traditional gate-dielectric material SiO_2 in sub-0.1 µm CMOS technology. It is however generally assumed that an ultra-thin SiO_2 layer is necessary between the Si substrate and an alternative dielectric material in order to match bondings and charges to each other and to reduce mechanical stresses and in that way to achieve a high level of charge carrier mobility.

As the following consideration shows, such a thin SiO_2 intermediate layer reduces the dielectric effectiveness of the substitute material. If we assume that the thickness $t_{high.k}$ of the alternative dielectric is to afford the same capacitance as an SiO_2 layer of the equivalent thickness t_{eq}, that gives:

$$\text{thigh-k} = (\text{khigh-k} / \text{kSiO2})\text{teq}, \qquad (1)$$

wherein k_{SiO2} is the dielectric constant of the SiO_2. As the SiO_2 intermediate layer represents a second capacitance C_{SiO2} connected in

series with the alternative dielectric, the resulting capacitance can be calculated as follow:

$$1/C_{res} = 1/C_{high\text{-}k} + 1/C_{SiO2}, \quad (2)$$

wherein $C_{high\text{-}k}$ is the capacitance of the dielectric layer. Using (1), that then gives the following for the equivalent thickness of the layer system t^s_{eq}, comprising a thin SiO_2 layer t_{SiO2} and the dielectric layer $t_{high\text{-}k}$,

$$t^s_{eq} = t_{SiO2} + (k_{SiO2} / k_{high\text{-}k})t_{high\text{-}k}, \quad (3)$$

It follows directly from (3) that the minimum attainable equivalent oxide thickness t^s_{eq} can never be less than the thickness t_{SiO2} of the SiO_2 layer. This therefore jeopardizes the increase in capacitance which is sought to be achieved with the use of a material with a high dielectric constant.

While a very high capacitance in respect of the layer, in the case of extremely slight leakage currents, is essential for use of the material in dynamic RAMs (DRAMs), a very high interface quality and charge carrier mobility in the channel are crucial for use of the material in MOSFETs.

Disclosure of the Invention

The technical object of the present invention is to provide a semiconductor component of the kind set forth in the opening part of this specification, with a sufficiently high capacitance and charge carrier mobility, even with particularly small dimensions. A further object of the invention is to provide a process for the production of such a component.

In regard to the semiconductor component that object is attained by a semiconductor component having a silicon-bearing layer and a praseodymium oxide layer, wherein arranged between the silicon layer and the praseodymium oxide layer is a mixed oxide layer containing silicon, praseodymium and oxygen, which is of a layer thickness of less than 5 nanometers.

The invention is based on the realization that a mixed oxide containing silicon, praseodymium and oxygen is suitable for combining the advantageous properties of the hitherto usual SiO_2/Si(001) interface with

those of the alternative dielectric praseodymium oxide (for example in the form of Pr_2O_3).

The mixed oxide which hereinafter is also referred to praseodymium silicate has a greater dielectric constant in comparison with silicon oxide. On the assumption that the mixed oxide layer is of the same thickness as an otherwise necessary silicon oxide intermediate layer between the silicon-bearing substrate and the praseodymium oxide, the minimum attainable equivalent oxide is reduced, in accordance with equation (3), by a factor which corresponds to the ratio of the dielectric constants of praseodymium silicate and silicon oxide.

The mixed oxide layer affords a high level of charge carrier mobility in the component according to the invention in accordance with the present state of knowledge by virtue of the fact that there are Si-O bonds and no Si-Pr bonds at the interface relative to the silicon-bearing layer. The Si-O bonds afford electrical properties as are known from the SiO_2/Si(001) interface.

Accordingly by means of the mixed oxide layer according to the invention it is possible to guarantee on the one hand a very high level of interface quality and on the other hand a sufficiently high capacitance. A transition from the silicon-bearing substrate to the dielectric is achieved, which has all the required properties.

In accordance with the foregoing, the thickness of the mixed oxide layer influences the capacitance of a capacitor structure which includes the silicon-bearing layer and the praseodymium oxide layer in a semiconductor component according to the invention. According to the invention the layer thickness is at a maximum 5 nm. The higher the value of the capacitance that is sought to be achieved for a component according to the invention, the correspondingly smaller should be the selected layer thickness of the mixed oxide layer.

Therefore in most cases small mixed oxide layer thicknesses are preferred. In an embodiment of the invention the mixed oxide layer involves a layer thickness of a maximum of 3 nm.

In an embodiment of the invention which is particularly preferred at the present time the mixed oxide layer is a pseudo-binary, non-stoichiometric alloy of the type $(Pr_2O_3)_x(SiO_2)_{1-x}$ or a silicate of that type.

The value of x has been found to be dependent inter alia on the layer thickness. In other words, in the case of components involving different thicknesses for the mixed oxide layer, the coeffients x differ. The coefficient x increases with the layer thickness. A detailed analysis of the composition of the mixed oxide, characterized by x, has revealed that the value x increases from 0.3 to 1 with thickness, in the layer thickness range up to 3 nm.

In a further embodiment of the invention the coefficient x increases between the silicon-bearing layer and the praseodymium oxide layer. In this embodiment the coefficient x increases within the mixed oxide layer.

In a preferred embodiment the silicon-bearing layer comprises doped or undoped silicon. It is however also possible to provide a doped or undoped silicon-germanium alloy in the silicon-bearing layer. When silicon-germanium alloy is used, nitrogen can additionally be incorporated into the silicon-bearing layer to achieve a high-quality interface.

In that case the silicon-bearing layer at the interface to the mixed oxide layer preferably involves a (001) orientation. A particularly high level of interface quality is achieved in that way.

The component according to the invention can preferably be in particular in the form of an MOSFET (metal oxide semiconductor field effect transistor) or in the form of a memory component in a RAM unit (random access memory) like a dynamic ROM (DROM).

In regard to the process aspect the object of the invention is attained by a production process for an electronic component with a step of depositing a praseodymium oxide layer on a silicon-bearing layer, wherein prior to said deposit step a step of depositing a mixed oxide layer containing silicon, praseodymium and oxygen is effected at a substrate temperature of less than 700°C.

The process according to the invention is based on the realization that the underlying object thereof is to be attained if it is possible for the alternative dielectric material praseodymium oxide Pr_2O_3 to be so grown on Si(001) that no SiO_2 intermediate layer occurs and also such a layer is not necessary to achieve a sufficiently high level of charge carrier mobility.

That is achieved by a mixed oxide layer being grown on the silicon-bearing layer. That mixed oxide layer contains silicon, praseodymium and oxygen.

It is of great significance in terms of the interface quality and thus the charge carrier mobility that no silicides are formed in the semiconductor component according to the invention at the interface to the substrate. Here use is inventively made of the fact that, in the temperature range up to 800°C, praseodymium ions are subjected to repulsion forces at the surface of the silicon-bearing substrate material so that Si-O bonds and not Si-Pr bonds occur there. In other words, no silicides are formed at the interface to the substrate. The Si-O bonds which are produced instead at the interface afford particularly good electrical properties as are known from the SiO_2/Si(001) interface.

Accordingly, a chemically reactive interface exists, comprising an Si-Pr mixed oxide of the form $(Pr_2O_3)_x(SiO_2)_{1-x}$, which is typically of a non-stoichiometric composition.

The upper temperature limit of 700°C which is predetermined in accordance with the invention prevents decomposition of structure elements of the component produced, in particular the mixed oxide layer itself.

Preferably the steps of depositing a mixed oxide layer and depositing a praseodymium oxide layer are effected in the form of deposition out of the gaseous phase. Particularly controlled growth of the layers is achieved in that way.

The above-mentioned deposit steps can be effected by means of molecular beam deposition (molecular beam epitaxy or MBE) or by means of chemical vapor deposition or CVD.

In a particularly preferred embodiment of the process according to the invention the step of depositing the mixed oxide layer is effected in an oxygen-bearing gas atmosphere. As will be described in greater detail hereinafter with reference to Figure 1, it has been found that the presence of oxygen in the gas atmosphere of the growth chamber is of great significance in regard to controlling the layer composition. Thus particularly when there is a lack of oxygen, silicon monoxide SiO is produced instead of silicon dioxide SiO_2. The provision of oxygen makes it possible to control the composition, that is to say the stoichiometry coefficient x of the silicate $(Pr_20_3)_x(SiO_2)_{1-x}$. A provision of oxygen is of great importance for the production of the Si-O bonds in the region of the interface by virtue of the high reactivity of silicon from the silicon-bearing layer and oxygen.

An oxygen-bearing gas atmosphere is also advantageous for deposit of the praseodymium oxide layer.

Preferably a material which contains praseodymium oxide in the form of Pr_6O_{11} or which even completely consist thereof is used as a starting material for the step of depositing the mixed oxide layer. The reduction of praseodymium oxide Pr_6O_{11} in the growth chamber provides for an oxygen partial pressure with which the layer growth takes place in the desired manner. In this embodiment the oxygen content of the gas atmosphere can be controlled by means of the temperature.

Preferably the step of depositing the mixed oxide layer is effected at a substrate temperature of less than 680°C, in particular between 600°C and 650°C. Particularly when using Pr_6O_{11} as starting material, it is possible in that temperature range to guarantee sufficient provision of oxygen which leads to the formation of the mixed oxide $(Pr_20_3)_x(SiO_2)_{1-x}$.

Brief Description of the Drawings

The invention is described in greater detail hereinafter with reference to two Figures of drawings in which:

Figure 1 shows a ternary phase diagram for the praseodymium-oxygen-silicon system, and

Figure 2 shows an embodiment of the semiconductor component according to the invention.

Detailed Description of the Invention

Figure 1 shows a ternary phase diagram for the praseodymium-oxygen-silicon system. That phase diagram was experimentally ascertained in the context of research work in connection with the present invention.

The phase diagram has three co-ordinate axes 10, 12 and 14 arranged in the form of an equilateral triangle. The elements praseodymium, oxygen and silicon are associated with the corner points of the equilateral triangle. The concentration of those elements corresponds there to the value 1. The concentration of the respective element falls along the sides of the triangle, to the value zero.

Silicon monoxide SiO is present with a silicon content 0.5. That point of the phase diagram is identified by reference numeral 16. Silicon dioxide SiO_2 is present with a silicon content of 0.33. That point of the phase diagram is identified by reference numeral 18. Along the co-ordinate axis 14 the phase contains exclusively praseodymium and oxygen and no silicon. The Figure also shows the point 20 at which praseodymium oxide is present in the form Pr_2O_3.

Various experimentally ascertained phases of the mixed oxide are illustrated within the triangle formed by the three co-ordinate axes 10, 12 and 14, in the form of squares. The experimental values were ascertained by means of photoelectron spectroscopy on the basis of samples grown in the temperature range of between 600 and 650°C. To ascertain their composition the samples were excited with synchrotron radiation and the

energy of the electrons emanating from the sample is recorded and analyzed. It is found that the samples ascertained, depending on the respective oxygen content involved, are on a quasi-binary section line 22 representing a mixed phase of praseodymium oxide Pr_2O_3 and silicon monoxide SiO, or on a quasi-binary straight section line 24 representing a mixed phase of praseodymium oxide Pr_2O_3 and silicon dioxide SiO_2. At a point 25 at which the section line 24 intersects the median perpendicular, leading from the apex to the base, of the triangular phase diagram a $(Pr_2O_3)_x(SiO_2)_{1-x}$ thortveitite structure was ascertained. At that point 25 of the phase diagram the proportion of silicon and praseodymium in the mixed oxide are equal.

The phase diagram in Figure 1 accordingly shows that it has been possible to produce a praseodymium silicate or a pseudo-binary, non-stoichiometric alloy $(Pr_2O_3)_x(SiO_2)_{1-x}$ with an adjustable proportion x of the praseodymium oxide Pr_2O_3.

Figure 2 shows a section of an embodiment of a semiconductor component 30 according to the invention with a silicon substrate 32 and a mixed oxide layer 34 adjoining same. At an interface 36 between the silicon substrate 32 and the mixed oxide layer 34 the substrate has a (001) surface. The mixed oxide layer is a $(Pr_2O_3)_x(SiO_2)_{1-x}$ layer wherein the coefficient x at the interface 36 is of a value 0.3 and at an interface 38 to an adjacent praseodymium oxide layer (Pr_2O_3) 40 it is of a value 1. A polysilicon layer 42 is arranged above the praseodymium oxide layer 40.

The substrate 32 is not shown in greater detail here in its internal structure. The component 30 which is here also shown only in respect of a section thereof can be for example an MOSFET or a memory element of a DROM memory.